REMARKS

Claims 1-29, all the claims pending in the application, stand rejected on prior art grounds. Applicants respectfully traverse the rejection based on the following discussion.

I. The Prior Art Rejections

Claims 1-29 stand rejected under 35 U.S.C. §102(e) as being anticipated by Swanstrom et al., hereinafter "Swanstrom" (U.S. Patent No. 5,872,942). Applicants respectfully traverse this rejection based on the following discussion.

A. The Rejection Based on Swanstrom

Applicants respectfully traverse this anticipation rejection principally because the only channels mentioned in Swanstrom are multimedia channels 602-606 (Figure 10, column 16, line 60-column 17, line 7) which are external to the bridge 106 (and are connected to the bridge by way of buses external to the bridge) and are not channels "in said bridge" as defined by independent claims 1, 10, and 20. In response to Applicants' previous arguments, the Office Action states that Figure 1 of Swanstrom illustrates a bridge 106 having a plurality of channels by arguing that each of the buses 104, 108, 120, and 130 can include multiple channels. However, the claimed invention is not concerned with whether the buses have multiple channels, but instead is directed to a structure having multiple channels in the bridge. In the claimed invention, the bridge (230 in Figure 2) includes multiple channels (319-325 illustrated in Figure 3). Further the claims define that each of the channels within the bridge is connected to a bus (such as the processor local bus, peripheral device bus, etc. as in claim 1). Applicants also note that there is no distinction between the bridge 106 shown in Figure 1 and the bridge 106 shown in Figure 10 of Swanstrom, and that Swanstrom merely describes the bridge 106 as being a conventional commercially available Intel bridge in column 7, lines 51-56.

It is Applicants position that the Office Action improperly equates the channels/buses (102, 108, 120, 130, 602, 604, 605) external to the bridge shown in Figures 1 and 10 of Swanstrom with the channels (319-325) in the inventive bridge shown in applicants Figure 3. The conventional channels that are external to the bridge do not perform the same function and are not equivalent to the claimed channels "in the bridge." Because of this and other reasons, as explained in greater detail below, it is Applicants position that the claimed invention is not taught (or even suggested by Swanstrom.

The Office Action states that Swanstrom discloses "a bridge having a plurality of channels" referring to the buses external to the bridge 104, 108, 120, 130, thereby indicating that there is no difference between the buses external to the bridge and the claimed channels in the bridge. However, Applicants submit that this interpretation is incorrect because independent claims 1, 10, and 20 explicitly distinguish between the channels in the bridge and the buses external to the bridge (e.g., independent claims 1, 10, and 20 define that the channels in the bridge are connected to different buses, which requires that the channels and the buses external to the bridge must be different components). Further, the specification (page 7, lines 13-18) clearly explains the differences between channels in the bridge and buses connected to the bridge (e.g., see Figure 2 illustrating buses connected to the bridge and Figure 3 illustrating channels in the bridge). Therefore, as detailed below, Applicants submit that the rejection should be withdrawn.

More specifically, with respect to the claim language distinguishing the channels in the bridge from buses external to the bridge, independent claims 1, 10, and 20 provide channel(s) "in said bridge." This claim language provides that the channels are in the bridge and are therefore different than the buses external to the bridge shown in Figures 1 and 10 of Swanstrom. Further, this language of the independent claims also explains that the bus is connected to the channel, thereby again demonstrating that the channels in the bridge are different structures from the buses external to the bridge. The dependent claims similarly define that the channels includes buffer memories, random access memory, and a multiplexor. These claims further distinguish the claimed channels from buses external to the bridge. Thus, Applicants submit that the independent claims and their dependent claims clearly provide that the channels in the bridge are

not equivalent to buses external to the bridge.

As mentioned above, the specification and drawings demonstrate that the channels in the bridge are different structures from the buses external to the bridge. For example, Figure 2 illustrates many buses connected to the input/output interfaces of the bridge 230 and Figure 3 illustrates a number of buses (319-325) in the bridge. Further, page 7, lines 13-18 of the specification describe that each dedicated channel is uniquely connected to a different bus. Therefore, notwithstanding the claim language discussed above, when the claims are read in light of the specification, it is clear that the buses external to the bridge and channels in the bridge are different devices.

Thus, it is Applicants position that the plain language of the claims and the specification defines that the channels in the bridge are different structures than the buses external to the bridge. Therefore, the Office Action's interpretation that the buses external to the bridge and channels in the bridge are equivalent is incorrect with respect to the structures defined by independent claims 1, 10, and 20. More importantly, because Swanstrom merely states that item 106 is a bridge (column 7, lines 46-62) without explaining any details of the bridge, Swanstrom cannot be said to teach or suggest different channels in the bridge being dedicated to different exterior devices as defined by independent claims 1, 10, and 20.

Further, the invention provides non-blocking communication through multiple reserved lanes in the bridge (e.g., channels 319-325) that are managed by an implicit protocol (e.g., buffers 314 and multiplexors 316). The invention avoids relying on handshaking signals that leads to blocking communications when a destination or a shared resource is overloaded. The virtual channel communication architecture (VCCA), shown in Applicants' Figures 2-4, provides application specific bus interface flow control, by coordinating the access of resource competing components using reserved lanes. The virtual channel scheduler module uses multiple FIFO buffers 314, dedicated to distinct virtual channels 319-325, to allow the invention to implement the required multiple reserved lanes. With the invention, transactions occurring on each port interface may be routed to adjacent ports without having to pass through a bus. Similarly, each port has a data-path dedicated to the processor local bus 206.

To the contrary, Swanstrom merely describes a conventional bridge 106 and does not explain any details about the bridge 106. More specifically, in column 7, lines 46-62, Swanstrom describes that the chipset logic 106 includes various bridge logic and includes arbitration logic 107. The chipset logic 106 is similar to the Triton chipset available from Intel Corporation, including certain arbiter modifications to accommodate the real-time bus of the present invention. A second level or L2 cache memory may be coupled to a cache controller in the chipset logic 106, as desired. The bridge or chipset logic 106 couples through a memory bus 108 to main memory 110. The chipset logic 106 includes a memory controller for interfacing to the main memory 110 and also includes the arbitration logic 107. The chipset logic 106 includes various peripherals, including an interrupt system, a real time clock (RTC) and timers, a direct memory access (DMA) system, and ROM/Flash memory. Other peripherals are comprised in the chipset logic 106, including communications ports, diagnostics ports, command/status registers, and non-volatile static random access memory (NVSRAM). The host/PCI/cache bridge or chipset logic 106 also interfaces to a local expansion bus or system bus 120.

Therefore, it is Applicants position that Swanstrom does not teach any details regarding the bridge 106 and therefore does not teach (or even suggest) that the "bridge includes a first channel dedicated to said processor local bus . . . a second channel dedicated to said peripheral device bus . . . a third channel dedicated to said memory unit; and . . . a fourth channel dedicated to said input/output unit," as defined by independent claim 1; that the bus, memory unit, and input/output unit are each "connected to a uniquely dedicated channel in said bridge"; as defined by independent claim 10; or a bridge that has "dedicated channels in said bridge, each uniquely connected to one or more of:" the bus, memory unit, input/output unit, and peripheral device, as defined by independent claim 20 . Therefore, Applicants submit that independent claims 1, 10, and 20 are patentable over the prior art of record. Further, dependent claims 2-9, 11-19, and 21-29 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention defined. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw these rejections.

II. Formal Matters and Conclusion

Applicants submit that claims 1-29, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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